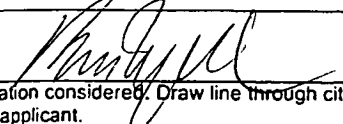


Substitute Form PTO-1449 (Modified) Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office		Attorney's Docket No. 01997-254002	Application No. 09/377,372
	Applicant Arvind Mithal et al.			
	Filing Date August 19, 1999		Group Art Unit 2731 2661	

U.S. Patent Documents							
Examiner Initial	Desig. ID	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
BN	AB	*EP 0329233	10/02/89	European Patent Office				
BN	AC	*EP 0 82902120 A2	09/12/97	European Patent Office				
	AD							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
BN	AE	Arvind et al., "Using Term Rewriting Systems to Design and Verify Processors", IEEE Micro Special Issue, May/June 1999
BN	AF	Babb et al., "Parallelizing Applications into Silicon", MIT Laboratory of Computer Science, April 1999
BN	AG	Cook et al., "Formal verification of explicitly parallel microprocessors", March 5, 1999
BN	AH	Gupta et al., "Hardware-software Co-synthesis for Digital Systems", Computer Science Laboratory, Stanford University, 1993
BN	AI	Liao et al., "An Efficient Implementation of Reactivity for Modeling Hardware in the System Design Environment", University of California at Irvine, 1997
BN	AJ	Mathews et al., "Microprocessor Specification in Hawk", 1998
BN	AK	Poyneer et al., "A TRS Model for a Modern Microprocessor", MIT Computation Structures Group Memo 408, June 25, 1998
BN	AL	Shen et al., "Design and Verification of Speculative Processors", MIT Computations Structures Group Memo 400 (B), 1998
BN	AM	Shen et al., "Modeling and Verification of ISA Implementations", MIT Computations Structures Group Memo 400 (A), 1998
BN	AN	Shen et al., "Using Term Rewriting Systems to Design and Verify Processors" Massachusetts Institute of Technology (June 1999)
BN	AO	Subrahmanyam et al., "Automated Synthesis of Mixed-Mode (Asynchronous and Synchronous) Systems AT&T Technical Journal (January 1991)
BN	AP	Windley, P., "Verifying Pipelined Microprocessors", Brigham Young University, 1995
BN	AQ	Windley, P., "Specifying Instruction-Set Architectures in HOL: A Primer", Brigham Young University, 1994

Examiner Signature 	Date Considered 11/15/04
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	